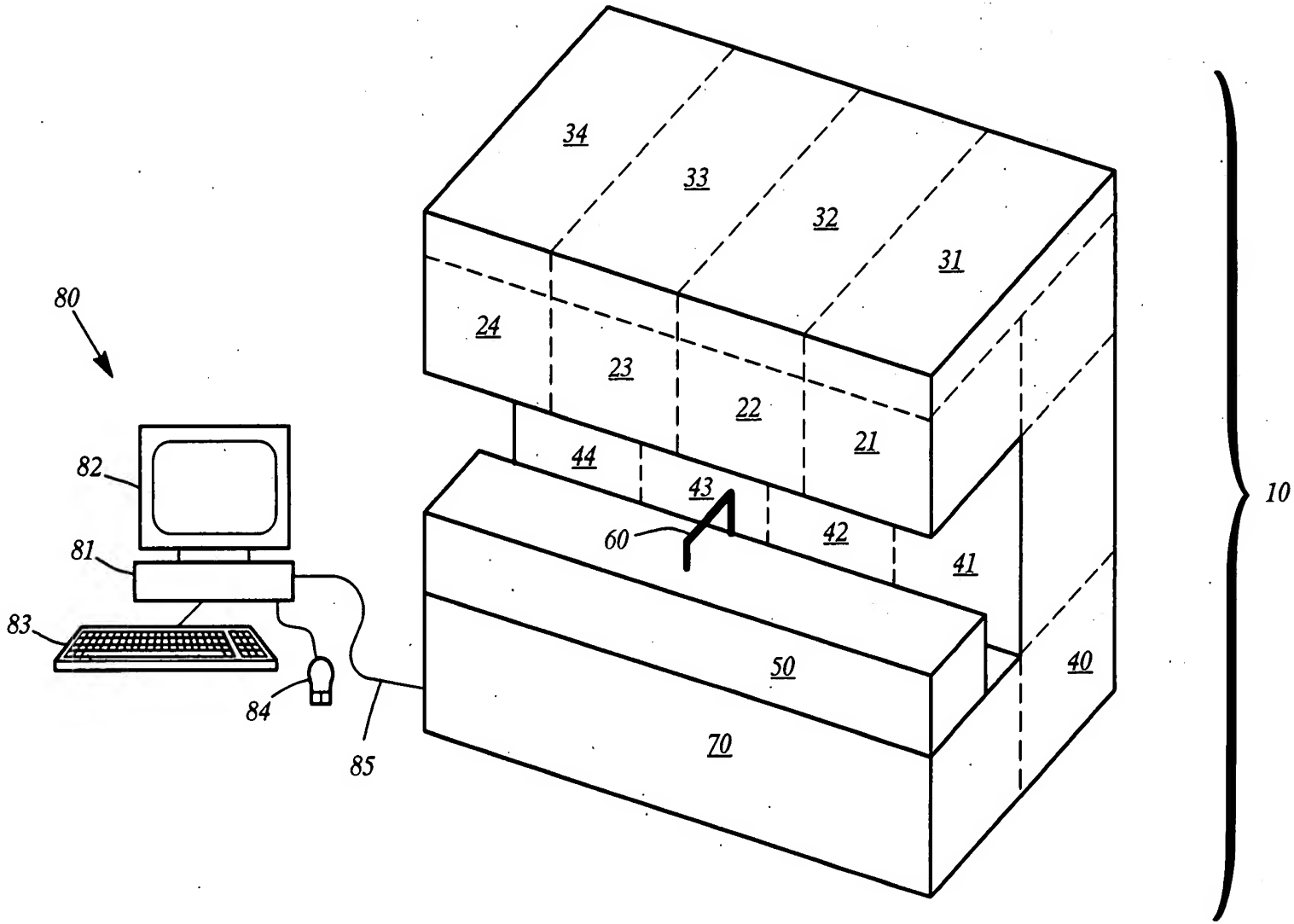

Figure 1

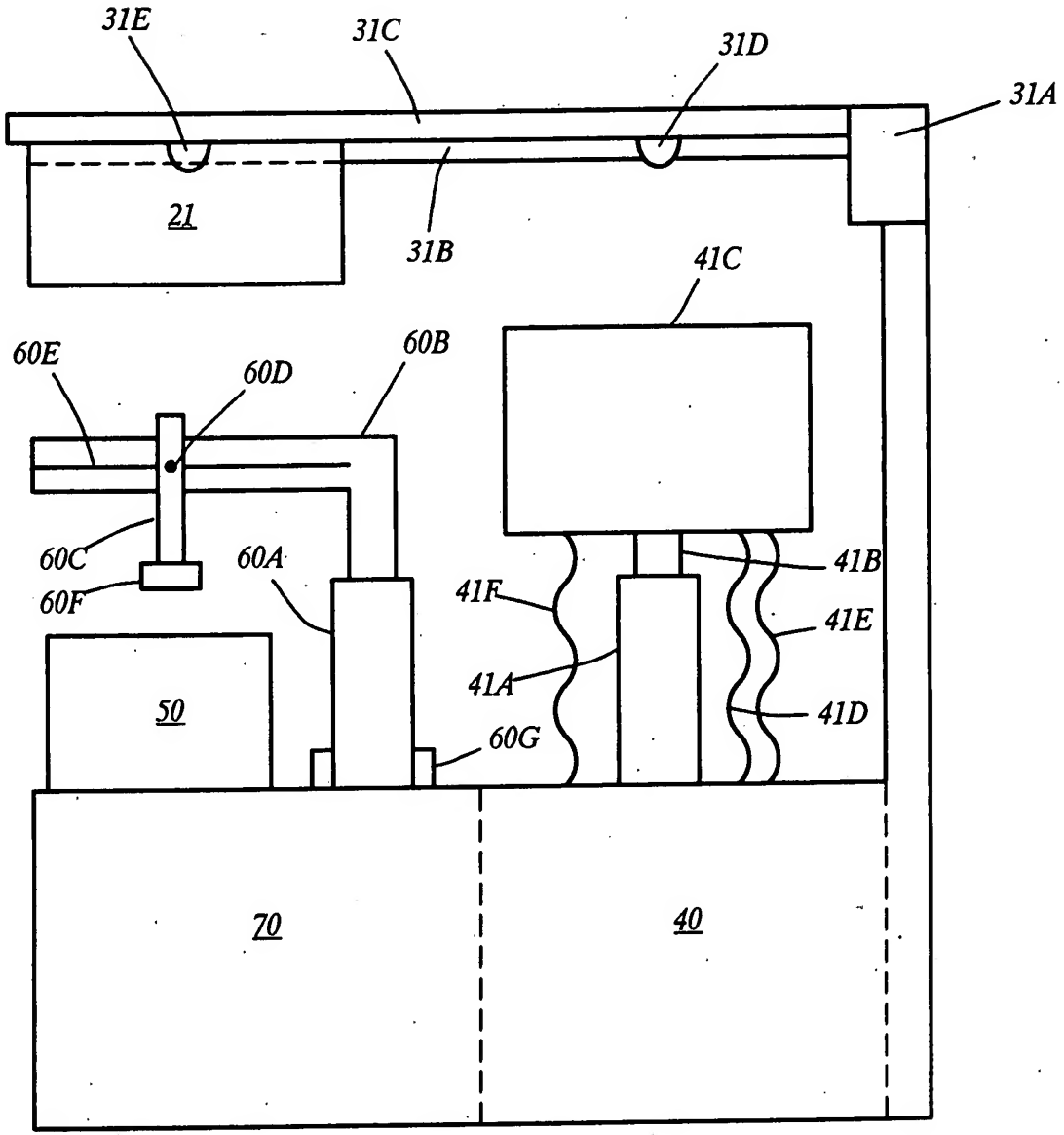
31E
31C
31D
31A
21
31B
41C
60E
60D
60B
60C
60A
60F
41F
41B
41E
41A
41D
50
60G
70
40

Figure 2

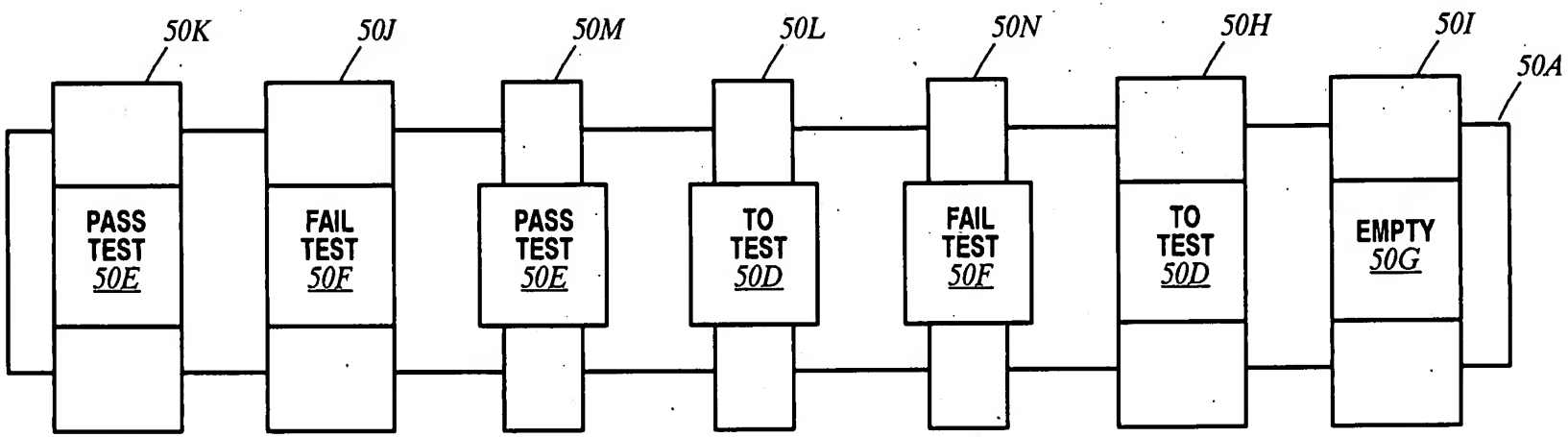

Figure 3A

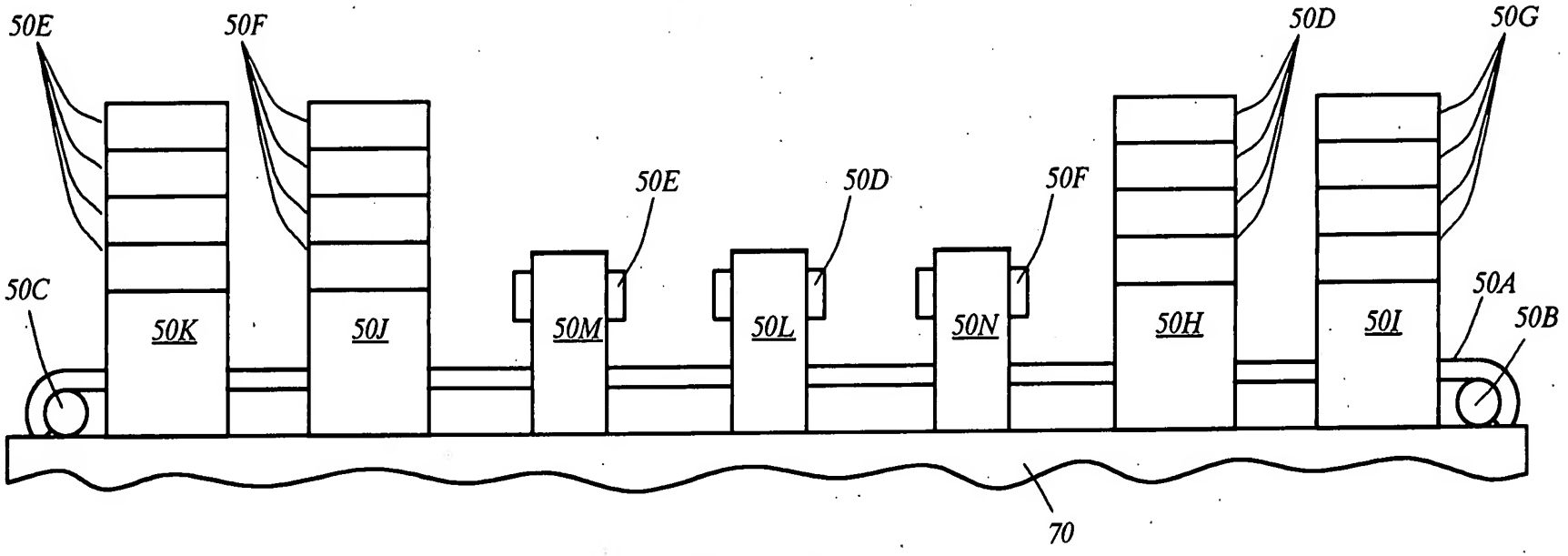

Figure 3B

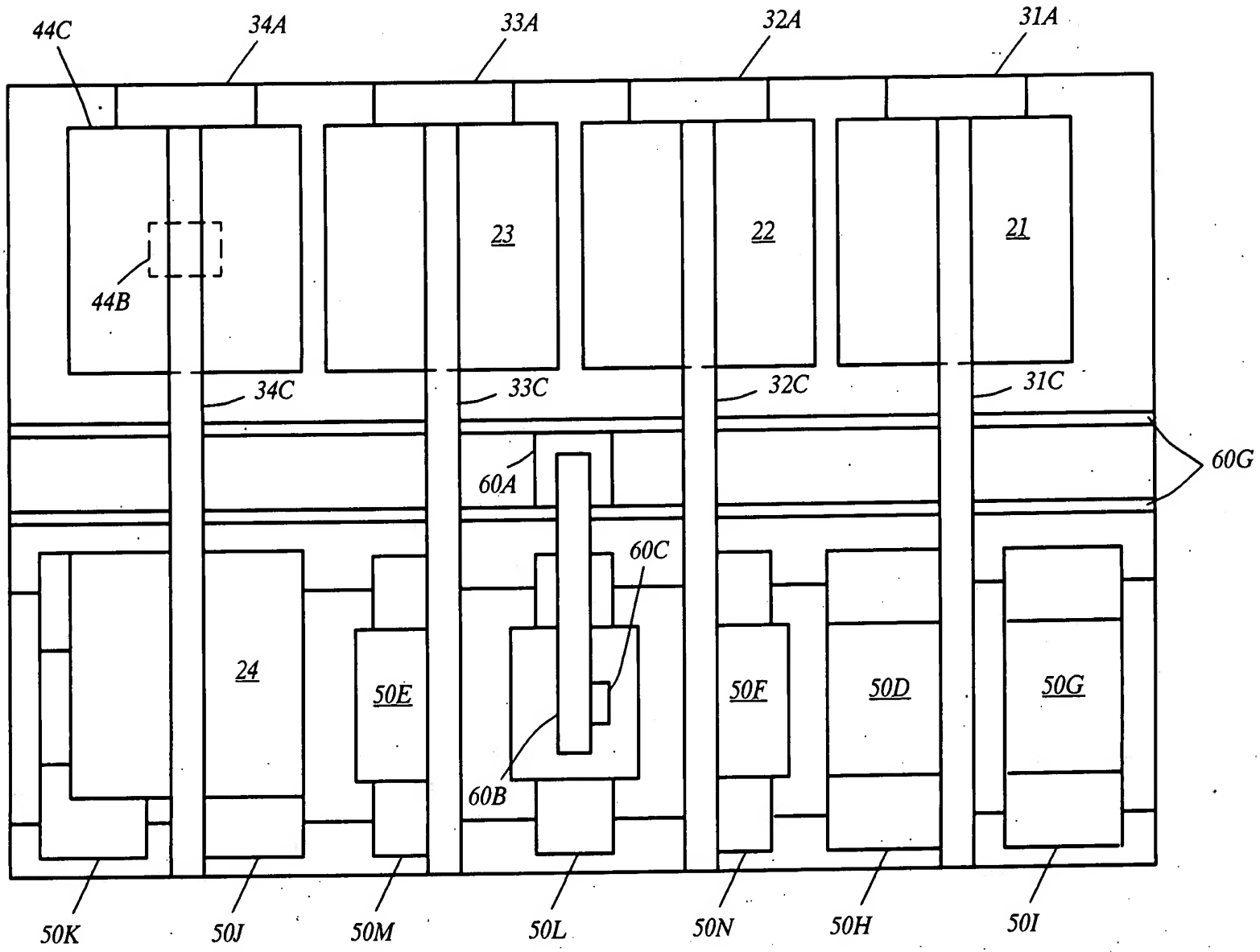
44C
34A
33A
32A
31A
23
22
21
44B
34C
33C
32C
31C
60G
60A
60C
24
50E
50F
50D
50G
60B
50K
50J
50M
50L
50N
50H
50I

Figure 4

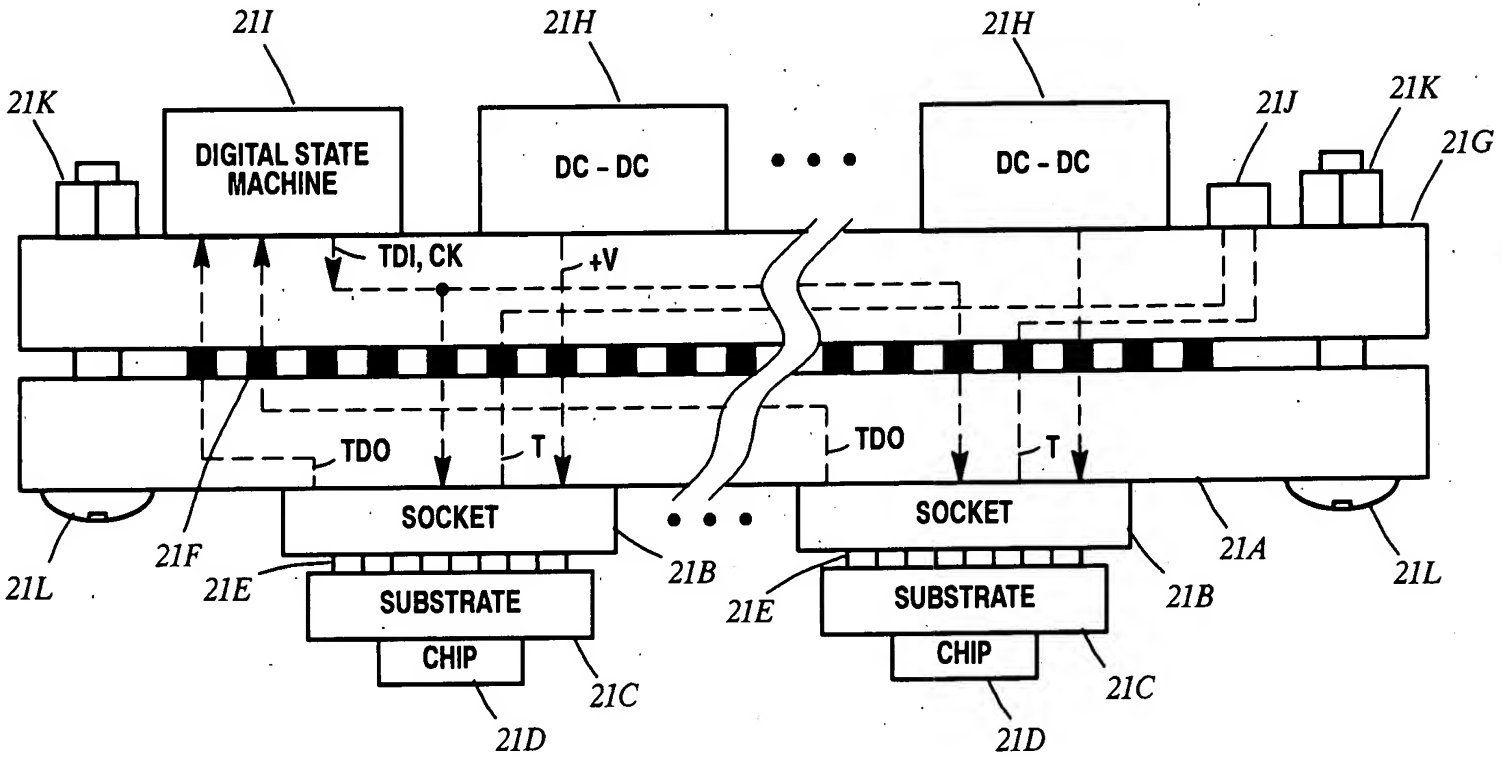
21I
21H
21H
21K
21J
21K
21G
DIGITAL STATE MACHINE
DC - DC
DC - DC
TDI, CK
+V
TDO
T
TDO
T
SOCKET
SOCKET
21L
21F
21E
21B
21A
21L
21E
21B
SUBSTRATE
SUBSTRATE
CHIP
CHIP
21C
21C
21D
21D

Figure 5

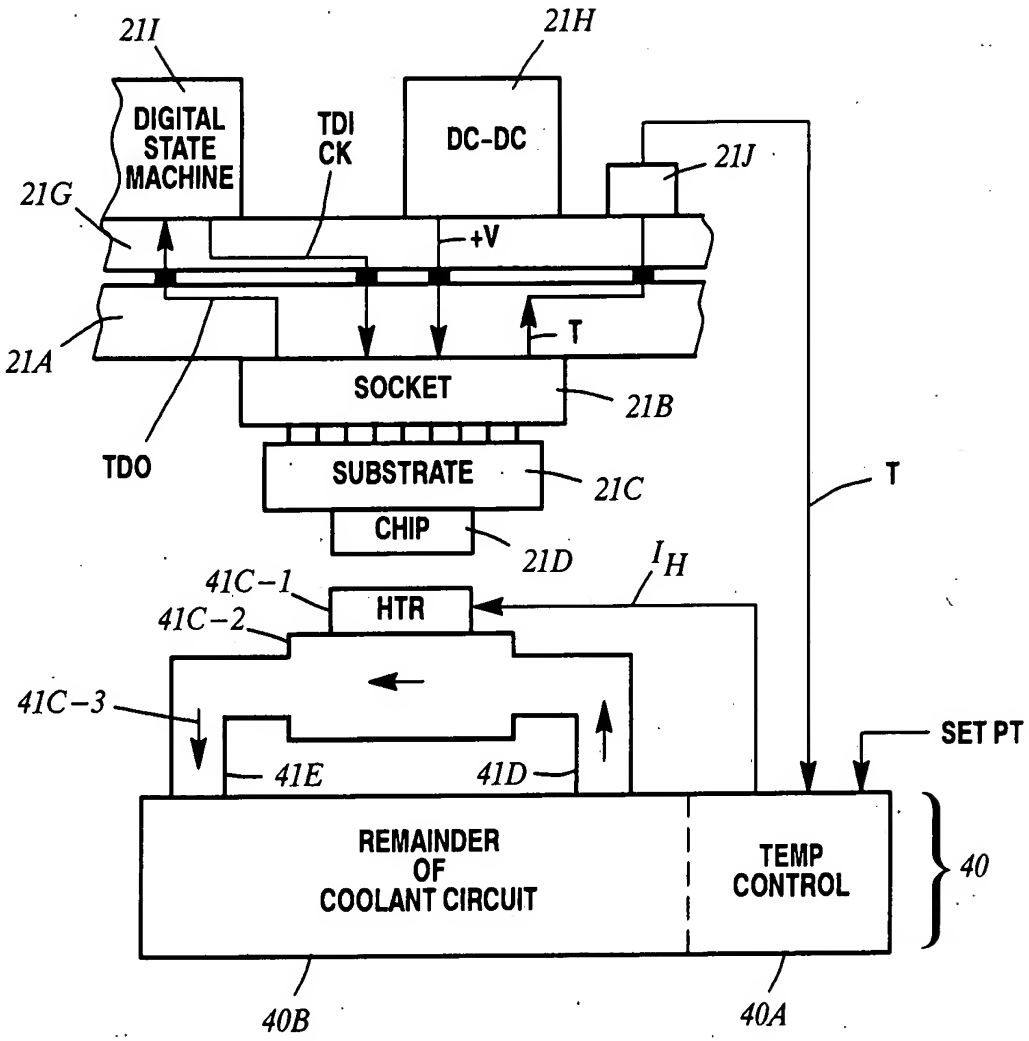
21I
21H
DIGITAL STATE MACHINE
TDI
CK
DC-DC
21J
21G
+V
T
21A
SOCKET
21B
TDO
SUBSTRATE
21C
T
CHIP
21D
I_H
41C-1
HTR
41C-2
41C-3
SET PT
41E
41D
REMAINDER OF COOLANT CIRCUIT
TEMP CONTROL
40
40B
40A

Figure 6

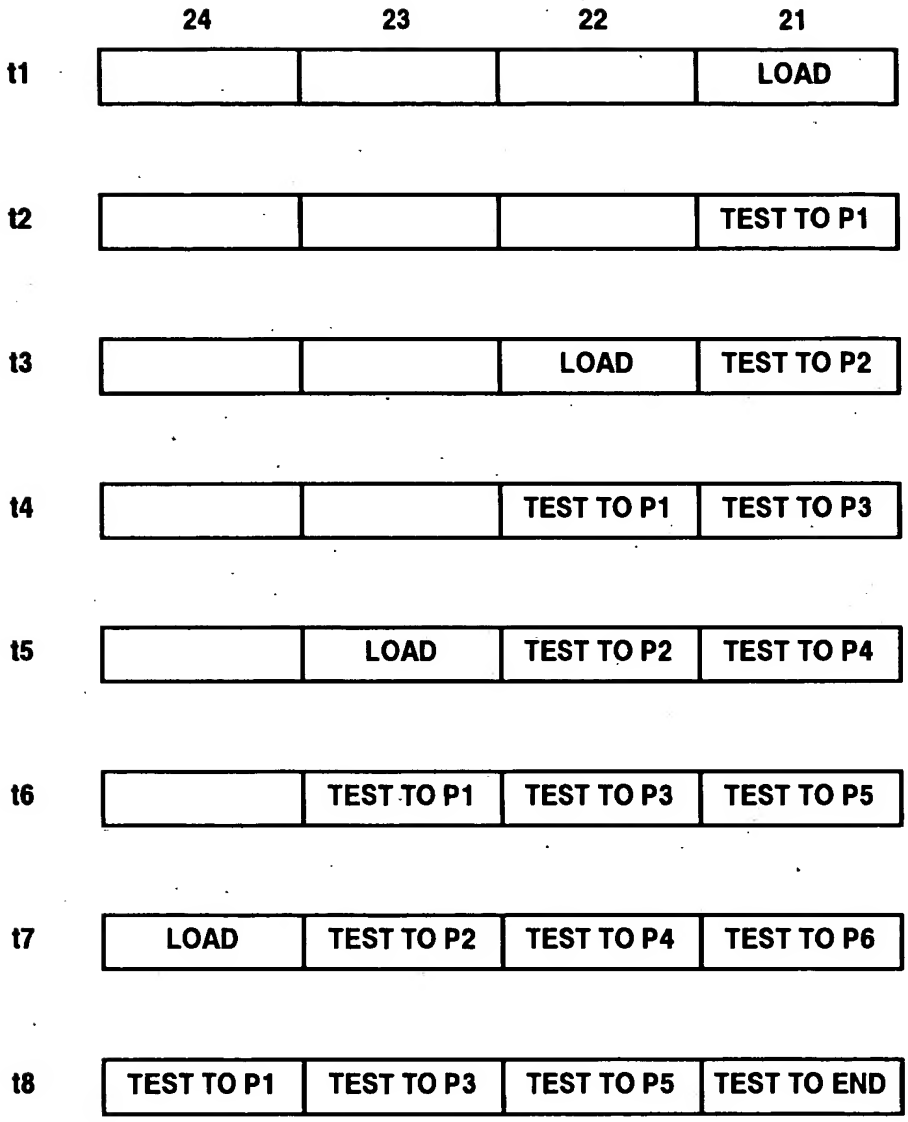
24
23
22
21
t1
LOAD
t2
TEST TO P1
t3
LOAD
TEST TO P2
t4
TEST TO P1
TEST TO P3
t5
LOAD
TEST TO P2
TEST TO P4
t6
TEST TO P1
TEST TO P3
TEST TO P5
t7
LOAD
TEST TO P2
TEST TO P4
TEST TO P6
t8
TEST TO P1
TEST TO P3
TEST TO P5
TEST TO END

Figure 7A

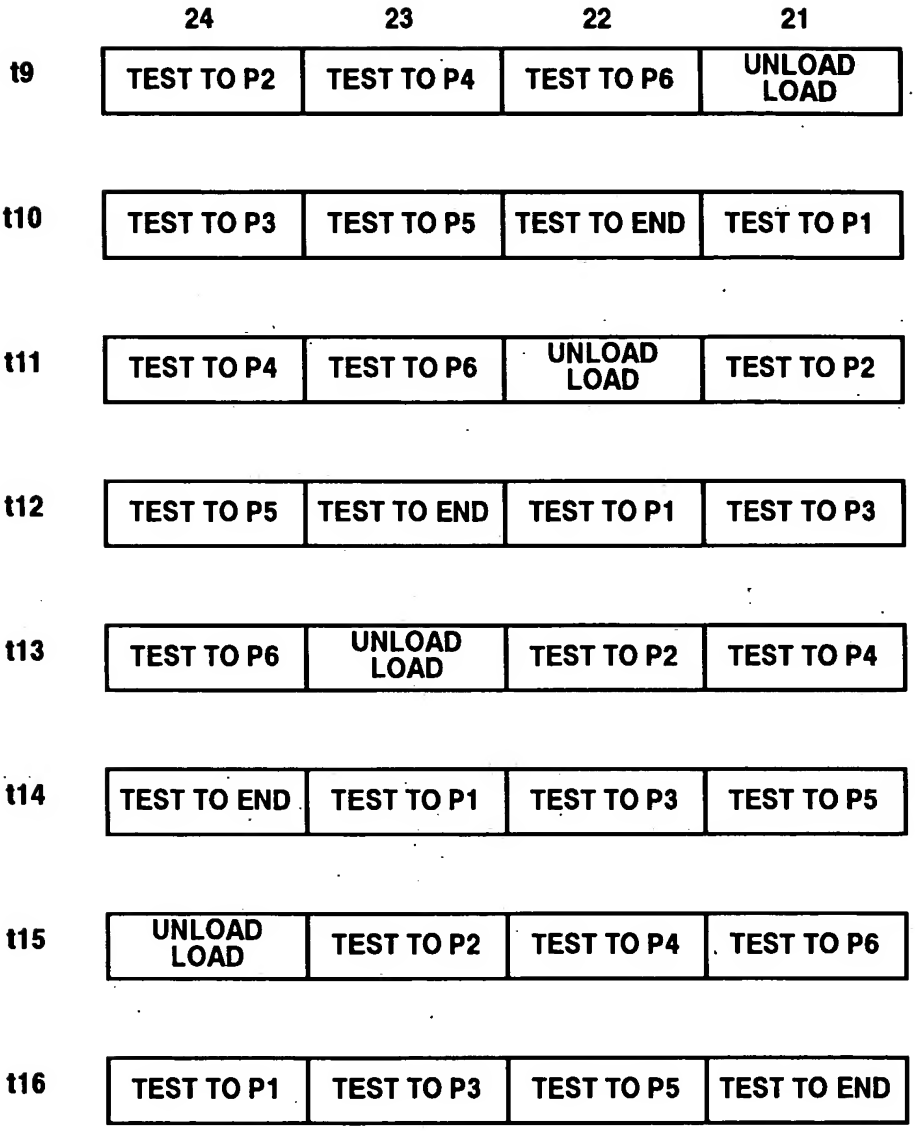
24
23
22
21
t9
TEST TO P2
TEST TO P4
TEST TO P6
UNLOAD LOAD
t10
TEST TO P3
TEST TO P5
TEST TO END
TEST TO P1
t11
TEST TO P4
TEST TO P6
UNLOAD LOAD
TEST TO P2
t12
TEST TO P5
TEST TO END
TEST TO P1
TEST TO P3
t13
TEST TO P6
UNLOAD LOAD
TEST TO P2
TEST TO P4
t14
TEST TO END
TEST TO P1
TEST TO P3
TEST TO P5
t15
UNLOAD LOAD
TEST TO P2
TEST TO P4
TEST TO P6
t16
TEST TO P1
TEST TO P3
TEST TO P5
TEST TO END

Figure 7B

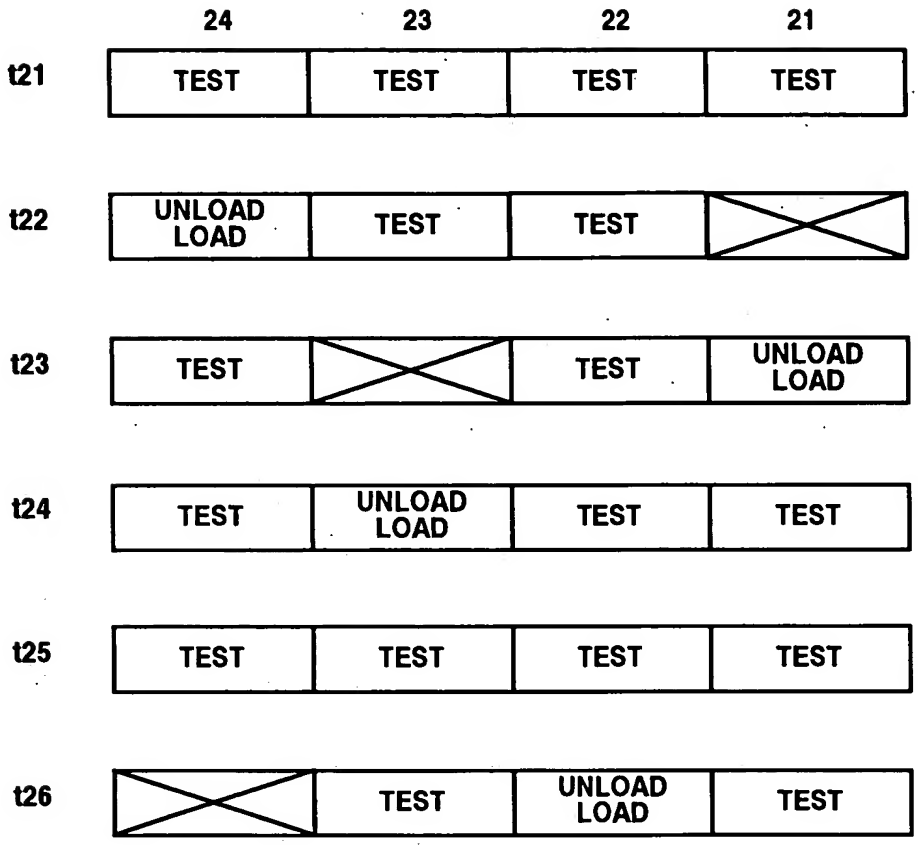
24
23
22
21
t21
TEST
TEST
TEST
TEST
t22
UNLOAD LOAD
TEST
TEST
t23
TEST
TEST
UNLOAD LOAD
t24
TEST
UNLOAD LOAD
TEST
TEST
t25
TEST
TEST
TEST
TEST
t26
TEST
UNLOAD LOAD
TEST

Figure 8

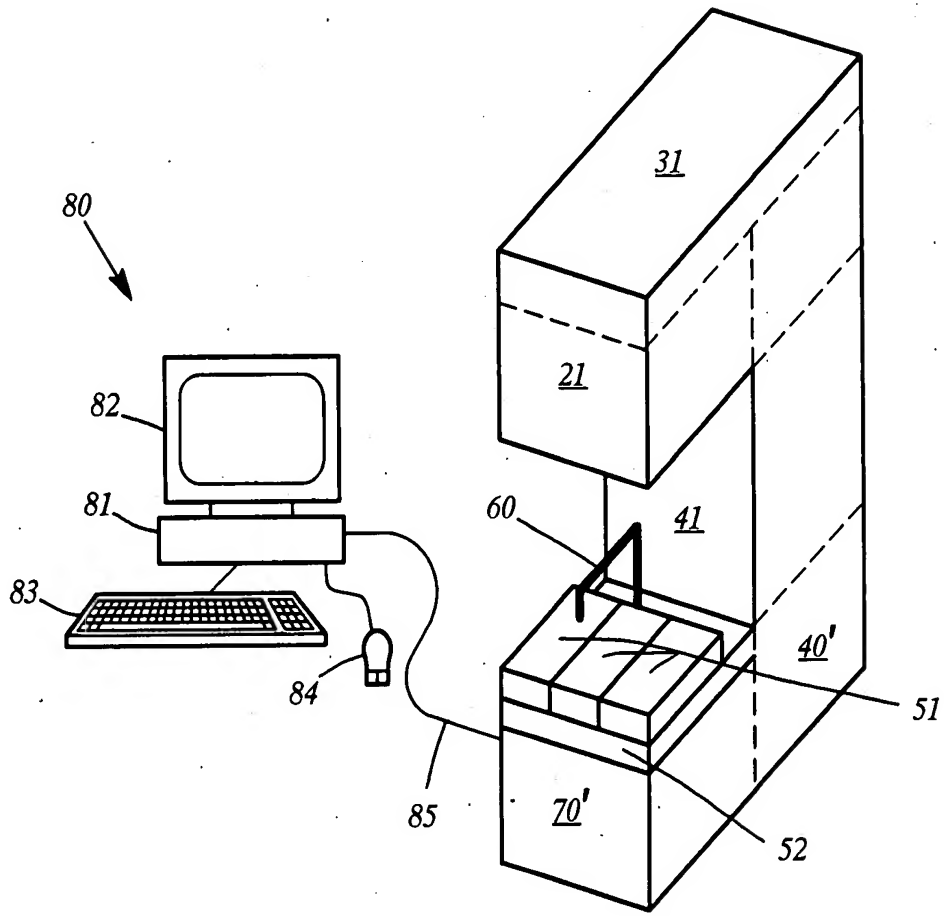

Figure 9

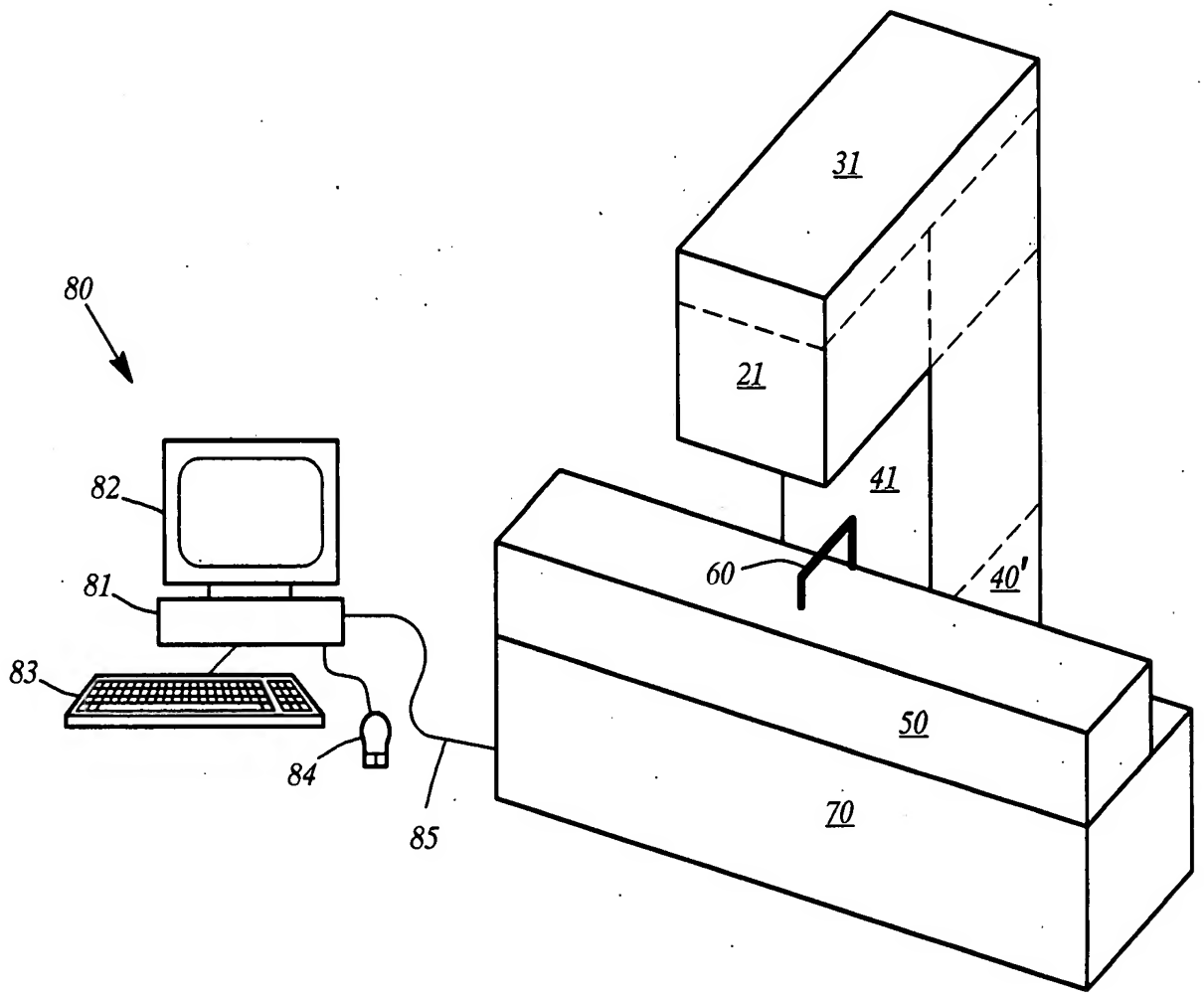

Figure 10

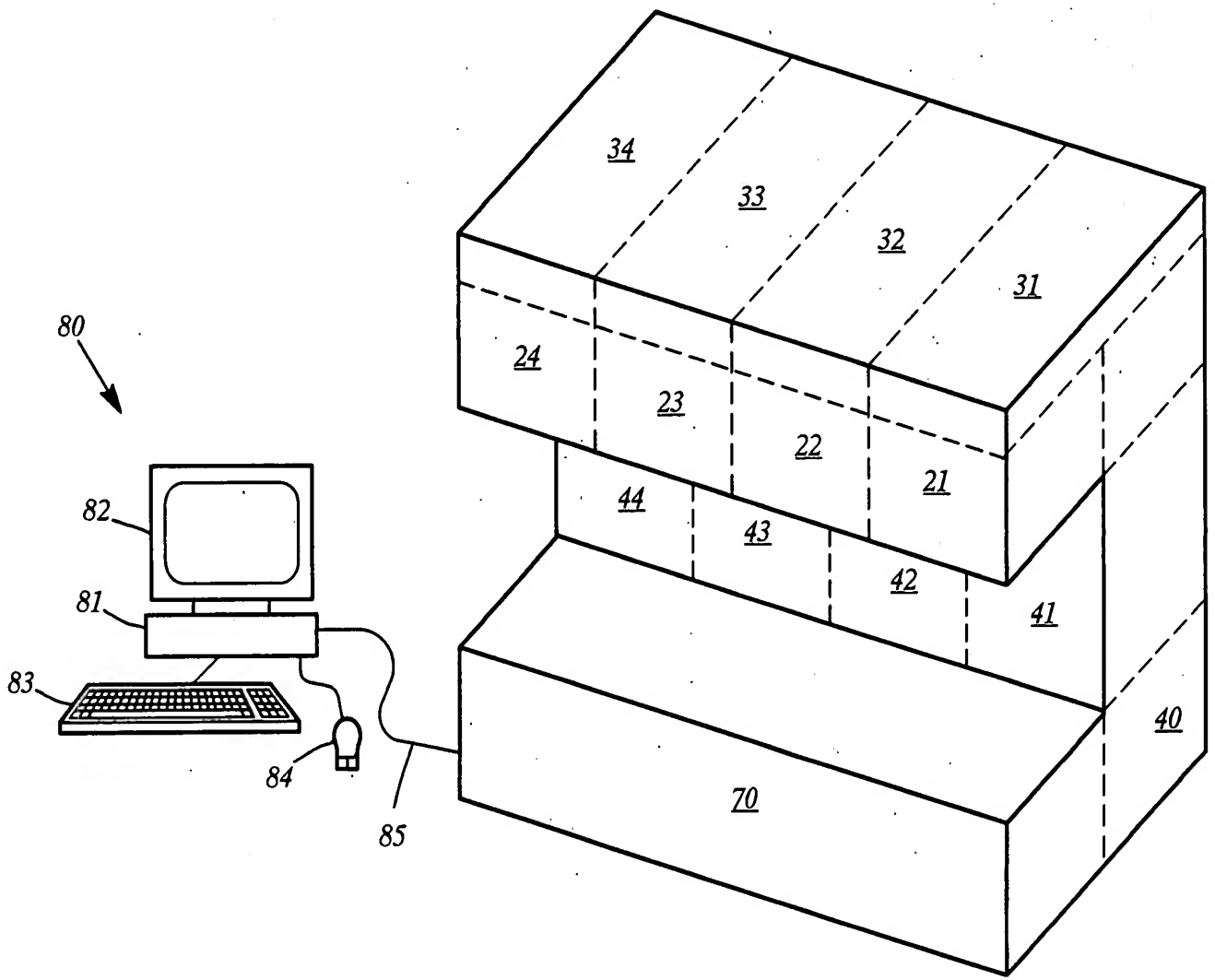

Figure 11

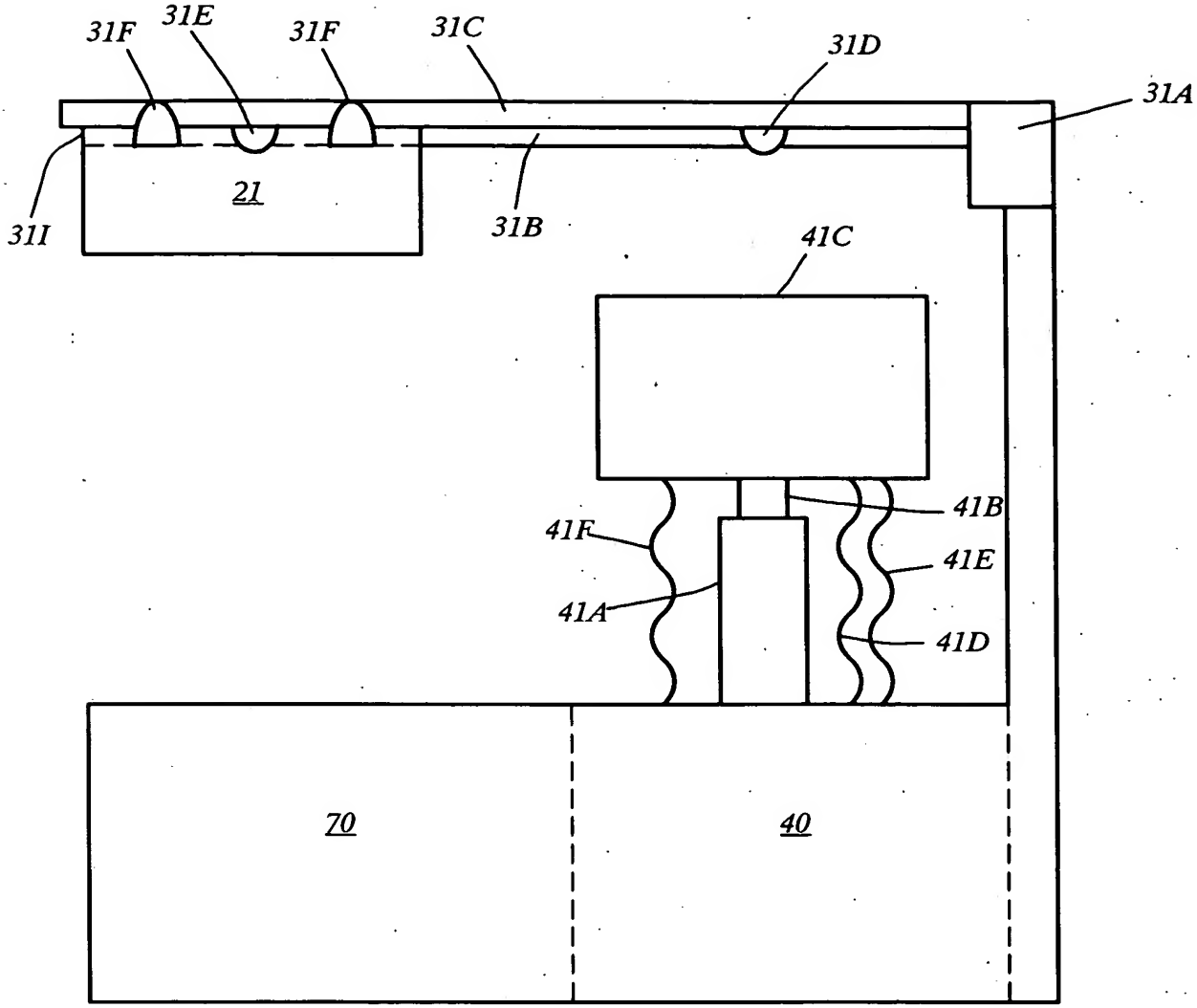

Figure 12

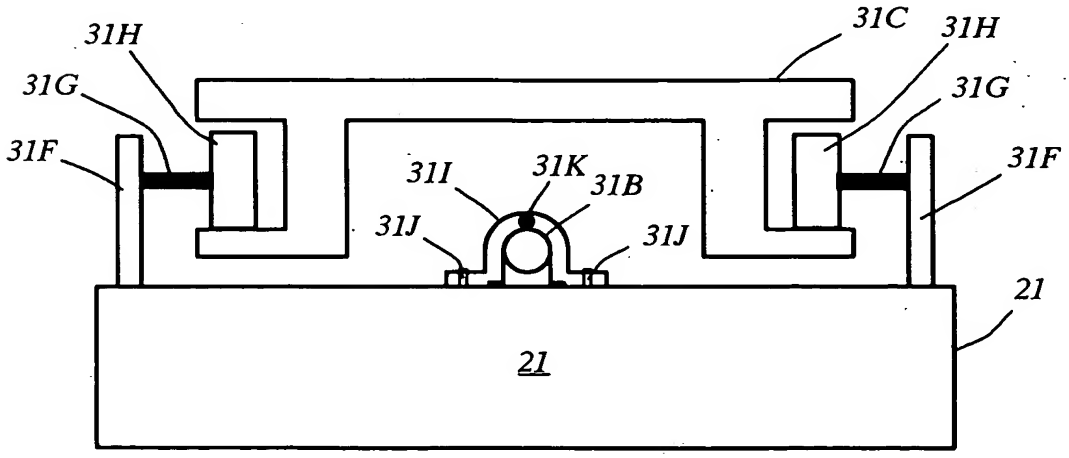

Figure 13

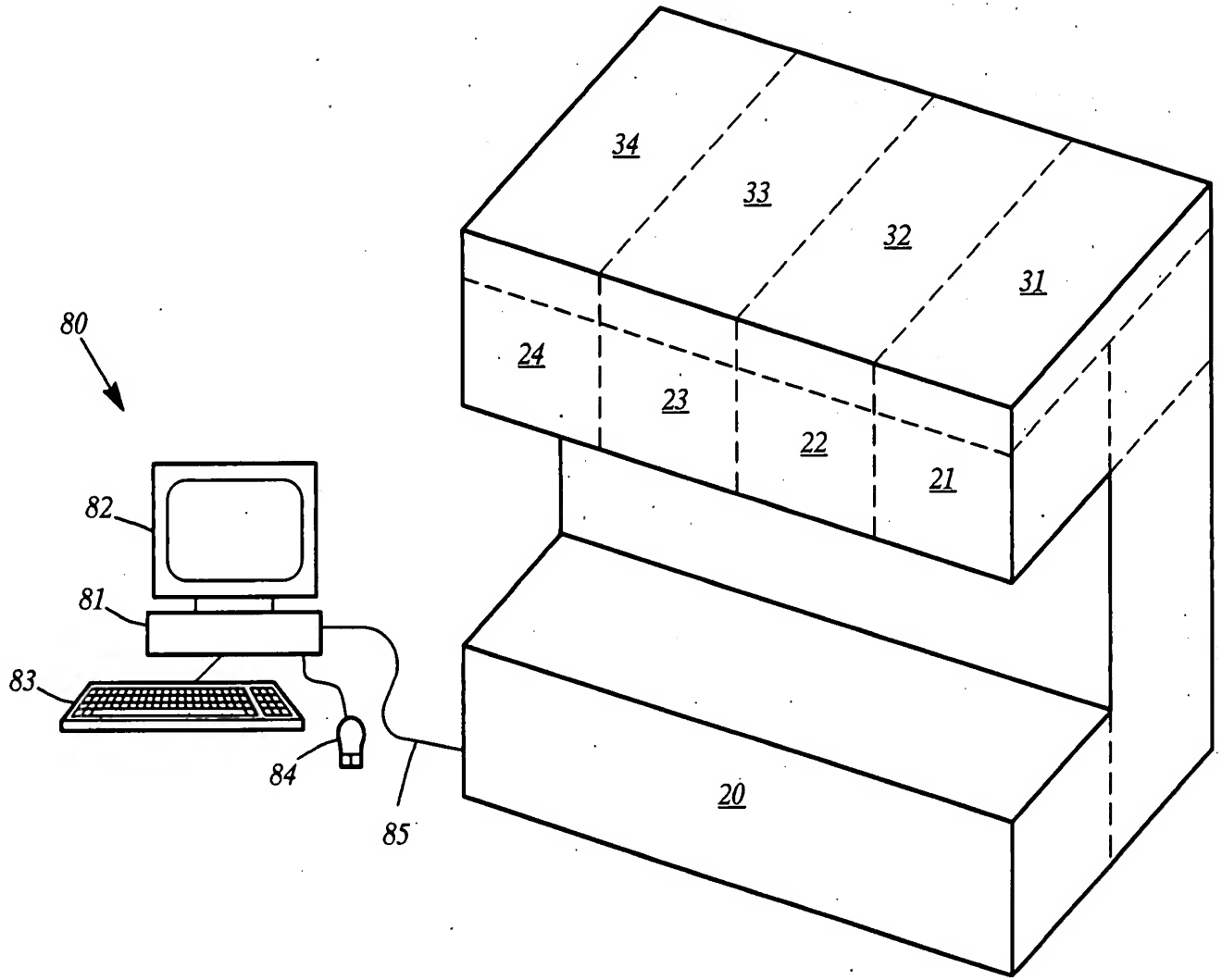

Figure 14

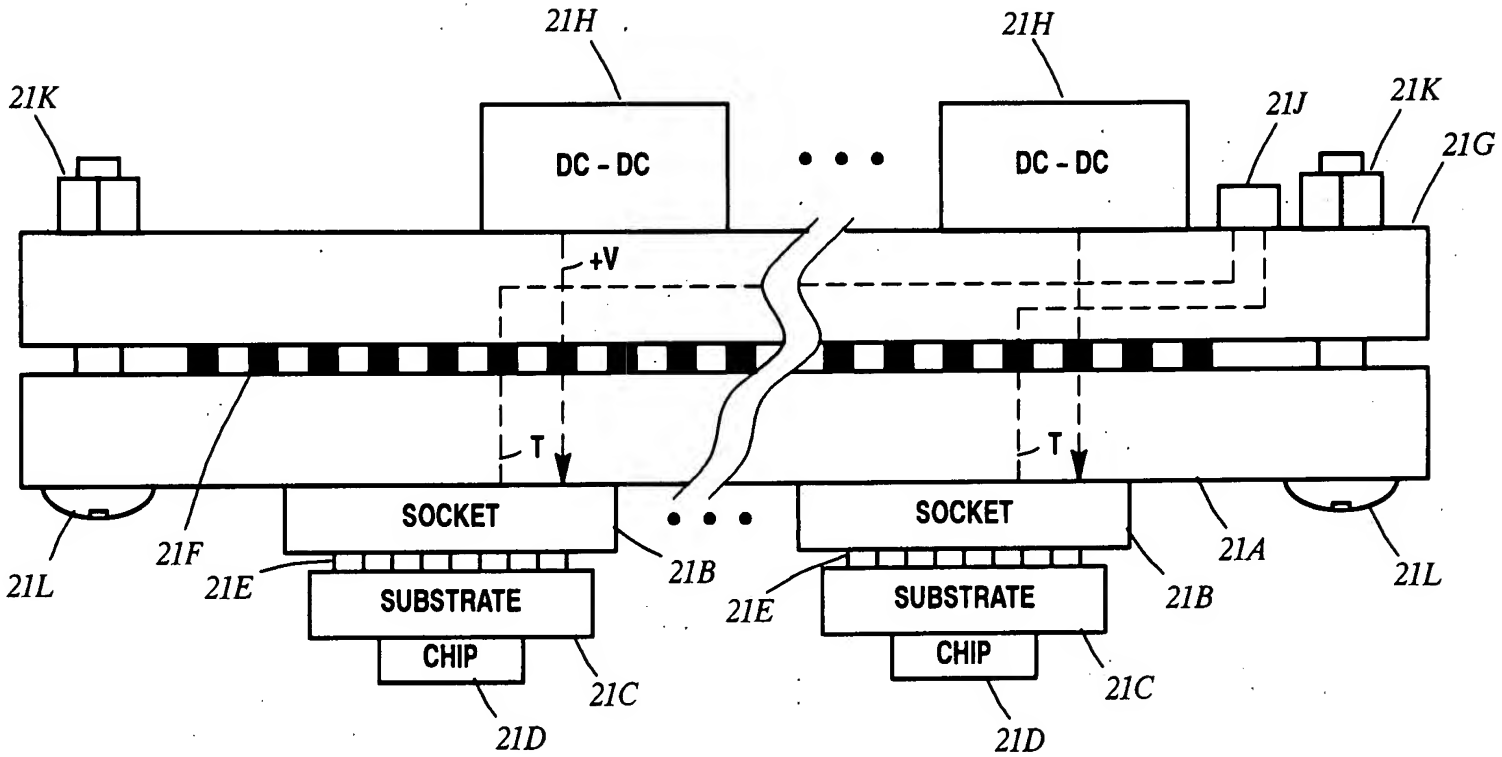
21H
21H
21K
21J
21K
21G
DC - DC
DC - DC
+V
T
T
SOCKET
SOCKET
21L
21F
21E
21B
21A
21L
21E
21B
SUBSTRATE
SUBSTRATE
CHIP
CHIP
21C
21C
21D
21D

Figure 15

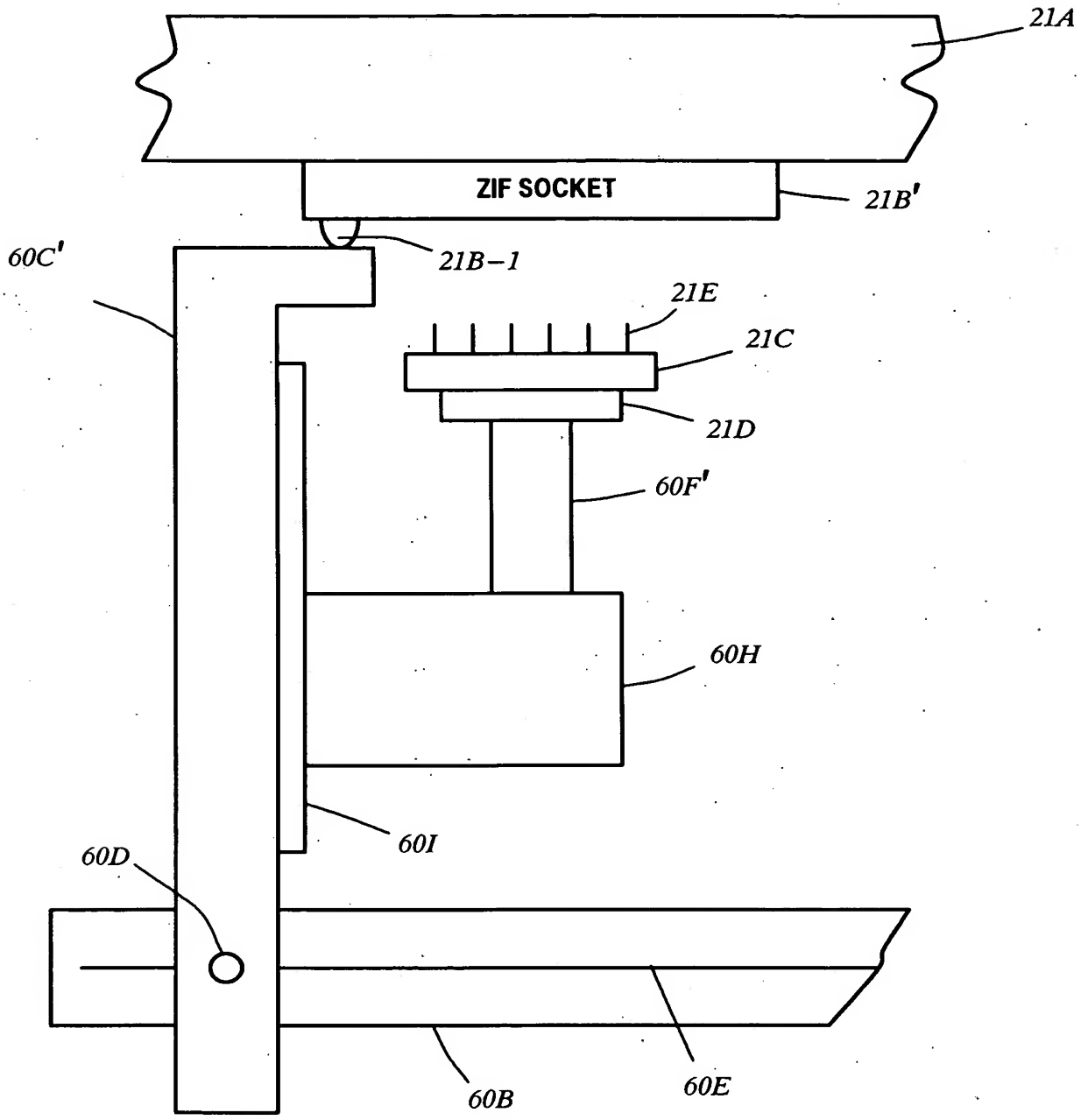

Figure 16